REMARKS

By this paper, Claims 15, 27, 35 to 37, 39 and 41 have been amended. After entry of the foregoing amendments, Claims 15, 27, 35 to 39 and 41 are in the application, with Claims 15, 27 and 37 being the pending independent claims. No new matter is believed to be added herein. Entry hereof and early passage to issue are respectfully requested.

Claim Rejections 35 U.S.C. §103

Claim 15 was rejected under 35 U.S.C. §103(a) over U.S. Pub. No. 2003/0127747 ("Kajiwara"), U.S. Pub. No. 2003/0146518 ("Hikita") and U.S. Pub. No. 2004/0115934 ("Broz"). Claim 35 was rejected under 35 U.S.C. §103(a) over Kajiwara, Hikita, Broz and U.S. Pat. No. 6,162,652 ("Dass"). Claims 27, 37 and 38 were rejected under 35 U.S.C. §103(a) over Kajiwara, U.S. Pat. No. 6,956,292 ("Fan"), Hikita and Broz. Claims 36 and 41 were rejected under 35 U.S.C. §103(a) over Kajiwara, Fan, Hikita, Broz and Dass. Claims 39 was rejected under 35 U.S.C. §103(a) over Kajiwara, Fan, Hikita, Broz and U.S. Pat. No. 6,104,461 ("Zhang"). Reconsideration and withdrawal of these rejections are respectfully requested.

Claim 15

Claim 15 is directed to a method for fabricating a circuit component. A semiconductor wafer is provided. A metal pad is provided over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. An exposed metallization structure is provided over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. After said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, a sputter etching process is performed with an argon gas.

The applied references, either alone or in combination, are not seen to disclose or suggest the foregoing combination of features of amended independent Claim 15.

The Office Action concludes that the combination of Kajiwara and Broz teaches the feature that "after said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, performing a sputter etching process with an argon gas," as recited in Claim 15 of the present application. The Office Action justifies that Kajiwara and Broz can be combined because "[b]oth references teach methods of surface cleaning a circuit component by sputter etching in forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of effectively removing contaminants and residues to facilitate probing during testing as well as to improve device performance by lowering contact resistance in subsequent processing steps." *See*, Office Action, page 4, lines 5-11.

Applicants respectfully disagree. Kajiwara teaches that "for the surface cleaning treatment in the flip-chip bonding step, the Au bump surface on the side of the chip is sputter etched by an Ar gas in an amount corresponding to 10 to 20 nm in the Au film……" *See,* Kajiwara, para. [0039], lines 40-43. Kajiwara's sputter etching process is therefore taught to be performed for flip-chip bonding to sputter etch an Au bump, but is not taught to be performed for testing. Even though Broz teaches that after performing a sputter etching process, a testing process can be performed in a wafer level process, (*see, e.g.,* Broz, para. [0016], lines 7, 28 and 29), Broz's testing process is believed not to be applicable to Kajiwara's flip-chip bonding process because multiple steps in a wafer-level process, typically performed before a die sawing step, are not believed to be readily transferred to a flip-chip bonding process, typically performed after the die sawing step. Furthermore, the considerations of an apparatus or mechanism for testing a chip package formed after a die sawing step are significantly different from those for testing a wafer provided before the die sawing step. The Office Action's proposed combination of Broz's wafer-level testing process with Kajiwara's flip-chip configuration therefore would change the principle of operation of Broz's wafer-level testing process.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959); MPEP §2143.01(VI).

The other cited references, Hikita, Fan, Dass and Zhang, individually or in combination, are not seen to remedy the above-discussed deficiency of Kajiwara and Broz. The Office Action does not cite Hikita, Fan, Dass or Zhang as teaching the above-discussed claim feature recited in Claim 15 of the present application.

Based on the above, at least the subject matter that after providing an exposed metallization structure comprising a metal bump configured for a package interconnect and prior to wafer testing of a semiconductor wafer, performing a sputter etching process, recited in Claim 15 of the present application, is believed to be patentably distinct over the cited references. Reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of Claim 15 are respectfully requested.

Claims 27 and 37

Claim 27 is directed to a method for fabricating a circuit component. A semiconductor wafer is provided. A metal pad over said semiconductor wafer is provided, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. An exposed metallization structure is provided over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. After said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, a ion milling process is performed with an argon gas.

Claim 37 is directed to a method for fabricating a circuit component. A semiconductor wafer is provided. A metal pad over said semiconductor wafer is provided, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. An exposed metallization structure is provided

directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump. After said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, an ion milling process is performed with an inert gas.

Claims 27 and 37 are believed to be allowable over the applied references at least because the subject matter that after providing an exposed metallization structure comprising a metal bump configured for a package interconnect and prior to wafer testing of a semiconductor wafer, performing an ion milling process, as recited in Claims 27 and 37 of the present application, is believed to be patentably distinct over the applied references for similar reasons presented above with respect to Claim 15. Reconsideration and withdrawal of the 35 U.S.C. §103(a) rejections of Claims 27 and 37 are therefore respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested. Reconsideration and withdrawal of the rejections of the dependent claims are respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the foregoing, Applicants submit that the claims are in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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